

REMARKS

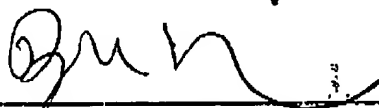
The Examiner has required restriction under 35 U.S.C. §121 between claims 33-61, drawn to a semiconductor device, classified in class 257, subclass 510, and claims 1-32, drawn to process for making semiconductor devices, classified in class 438, subclass 22+. Applicant hereby elects without traverse claims 1-32 for prosecution on the merits. Accordingly, claims 33-61 have been canceled without prejudice.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made.**"

In view of the foregoing, allowance of claims 1-32 is requested. The Examiner is requested to phone the undersigned in the event that the next Office Action is one other than a Notice of Allowance. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: October 26, 2001

By: 
Frederick M. Fliegel, Ph.D.
Reg. No. 36,138

FAX COPY RECEIVED

JUN 28 2002

TECHNOLOGY CENTER 2800

Version with markings to show changes made ✓

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/652,550
Filing Date August 31, 2000
Inventor Keiji Jono et al.
Assignee Micron Technology, Inc. and KMT Semiconductor, LTD
Group Art Unit 2811
Examiner T. Tran
Attorney's Docket No. KM1-001
Title: Methods of Forming an Isolation Trench in a Semiconductor, Methods
of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods
of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated
Transistor, Trench Isolation Structures Formed in a Semiconductor,
Memory Cells and DRAMS

37 CFR § 1.121(b)(1)(iii) AND 37 CFR § 1.121(c)(1)(ii)
FILING REQUIREMENTS TO ACCOMPANY RESPONSE TO
OCTOBER 12, 2001 OFFICE ACTION

Deletions are bracketed, additions are underlined.

In the Claims

Claims 33-61 have been canceled.

END OF DOCUMENT

FAX COPY RECEIVED

JUN 28 2002

TECHNOLOGY CENTER 2800

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application Serial No. 09/652,550
Filing Date August 31, 2000
Inventor Keiji Jono et al.
Assignee KMT Semiconductor, LTD
Group Art Unit 2811
Examiner Thien Tran
Attorney Docket No. KM1-001
Title: Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming
an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation
Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures
Formed in a Semiconductor, Memory Cells and DRAMS

FAX COPY RECEIVED

Assistant Commissioner for Patents
Washington, D.C. 20231

JUN 28 2002

TECHNOLOGY CENTER 2800

CERTIFICATE OF FACSIMILE TRANSMISSION UNDER 37 CFR 1.8

I hereby certify that the following papers are being facsimile transmitted to
the Patent and Trademark Office at (703) 872-9318 on the date shown below:

1. Certificate of Facsimile Transmission
2. Transmittal Form
3. Response to 06/25/02 Teleconference With Examiner
4. Postcard which accompanied Response to 10/12/01 Office Action
w/PTO receipt stamp
5. Transmittal Form dated 10/26/01 which accompanied said Response
to 10/12/01 Office Action
6. Response to 10/12/01 Office Action
7. Version With Markings to Show Changes Made

Dated: 06/27/02

By: Pat Palmer
Pat Palmer
Telephone No. (509) 624-4276
Facsimile No. (509) 838-3424

NUMBER OF PAGES IN FACSIMILE: 19